REMARKS

The following is intended as a full and complete response to the Office Action dated July 30, 2008, having a shortened statutory period for response set to expire on October 30, 2008. The Examiner rejected claims 1-5, 7, and 9-37 under 35 U.S.C. §112 as failing to comply with the written description requirement. The Examiner rejected claims 1-5, 7 and 9-37under 35 U.S.C. § 103(a) as being unpatentable.

Rejections under Double Patenting

The Examiner provisionally rejected claims 1-14, 16, 18, 22-23, 25, and 31-35 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, 5, 7-8, 15, 20, 23, 27, and 30 of co-pending Application No. 10/715,370 and claims 2, 8, and 19 of co-pending Application No. 10/715,440. Applicants acknowledge the double patenting rejection made in the Office Action and respectfully request that the rejection be held in abeyance until the pending claims are in condition for allowance. At such time, an appropriate terminal disclaimer will be filed.

Rejections under 35 U.S.C. § 112

The Examiner rejected claims 1, 25 and 31 and dependent claims 2-5, 7, 9-24, 26-30 and 32-37 under 35 U.S.C. § 112 as failing to comply with the written description requirement. Claims 1, 25 and 31 recite the limitations of "Data Movement Engine (DME) configured to transfer physics simulation data between the PPM and at least one PPU internal memory in response to commands received from the PCE and to initiate context switches relative to one or more other system elements." In the rejection, the Examiner states that the specification discloses that the context switches occur relative to only DME and the Floating Point Engine (FPE) and, therefore, the scope of the limitation is greater than the associated disclosure in the specification. However, the specification clearly discloses that the context switches occur relative to the data banks IEM 52 and IER 53. These data banks constitute the "one or more other system elements" recited in the claims. The specification also makes clear that the DME and the FPE can then access these data banks, consistent with the dependent claims, such as claims 14 and 15 (see generally page 19, lines 9-13 of the specification). Based on

the disclosure in the specification, Applicants respectfully request the withdrawal of the § 112 rejections of the claims 1, 25 and 31 and dependent claims 2-5, 7, 9-24, 26-30 and 32-37.

The Examiner also rejected claim 14 and dependent claims 15-18 and 20-21 under 35 U.S.C. § 112 as failing to comply with the written description requirement. Applicants have amended claim 14 to overcome the rejection, and therefore, respectfully request the withdrawal of the § 112 rejection of the claim 14 and dependent claims 15-18 and 20-21.

Rejections under 35 U.S.C. § 103(a)

Claims 1-4, 7, 9-15, 18-19, 22-23, 25-27, 29-31, and 34 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Van Hook (U.S. 6,342,892 B1) in view of Bishop (SPARTA: Simulation of Physics on a Real-Time Architecture). Claim 5, 32-33, and 35-36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Van Hook (U.S. 6,342,892 B1) in view of Bishop and Intel (Intel PCI and PCI Express). Claims 16-17 and 20-21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Van Hook in view of Bishop and Dakhil (U.S. 6,341,318). Claims 24 and 37 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Van Hook in view of Bishop and Shiell (U.S. 6,317,820).

Claim 1 recites the limitations of a Physics Processing Unit (PPU) configured to provide force and collision computations on real-time physics simulation data, where the PPU includes (i) a PPU Control Engine (PCE) configured to control a physics simulation and to communicate with a PPU software driver executing on the Central Processing Unit (CPU). Neither Van Hook nor Bishop teaches or suggests these limitations.

Van Hook discloses a video game system having a central processing unit (CPU) and a coprocessor that handles audio and video signals through a signal processor. The coprocessor in Van Hook includes various sub-processors, such as a signal processor and a CPU interface. The CPU interface acts as a gateway for communication between the coprocessor and the main processor (see Van Hook, column 15, lines 48-50). The Examiner appears to equate the CPU interface disclosed in Van Hook to the claimed PCE. However, the CPU interface disclosed in Van Hook

simply transmits commands received by the main processor to the various sub-processors. The CPU interface in Van Hook does not control the processing of the commands received by the main processor and does not communicate with a coprocessor software driver executing on the main processor. As is expressly recited in claim 1, the PCE is configured to control a physics simulation and to communicate with a PPU software driver executing on the CPU. Thus, the parallel between the CPU interface taught in Van Hook and the claimed PCE simply cannot be made.

The Examiner also compares the signal processor within the coprocessor in Van Hook to the claimed PCE. The signal processor in Van Hook is a processor that executes audio and graphics tasks (see Van Hook, column 15, lines 30-32). The signal processor in Van Hook receives commands from the CPU interface and executes those commands. The signal processor does not communicate with a coprocessor software driver executing on the CPU, as recited in claim 1. Thus, the parallel between the signal processor taught in Van Hook and the claimed PCE simply cannot be made.

Bishop discloses an application-specific integrated circuit that can accelerate physics modeling in conjunction with a CPU. The Examiner relies on Bishop only to demonstrate a Physics Processing Unit (PPU). Thus, Bishop fails to cure the deficiencies of Van Hook.

As the foregoing illustrates, the combination of Van Hook and Bishop fails to teach or suggest each and every limitation of amended claim 1. In sum, the combination lacks both the structure and the function recited in claim 1. Therefore, amended claim 1 and claims 2-4, 6-15, 18-19, and 22-23, dependent thereon, are in condition for allowance.

With respect to claims 5, 17, 20, 21, and 24, Intel, Dakhil, Shiell, and Telekinesys all fail to cure the deficiencies of Van Hook and Bishop set forth above with respect to amended claim 1. Therefore, no combination of the cited references can teach or suggest each and every limitation of these dependent claims. For this reason, claims 5, 17, 20, 21, and 24 are also in condition for allowance.

Claims 25 and 31 recite limitations similar to those recited in claim 1 and are therefore allowable for at least the same reasons as allowable claim 1. Since claims

26-30 depend on claim 25, and claims 32-37 depend on claim 31, these claims are also in condition for allowance.

CONCLUSION

Based on the above remarks, Applicants believe that he has overcome all of the objections and rejections set forth in the Final Office Action mailed July 30, 2008 and that the pending claims are in condition for allowance. If the Examiner has any questions, please contact the Applicants' undersigned representative at the number provided below.

Respectfully submitted,

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